3-Dimensional Devices:

Models and Design Tools

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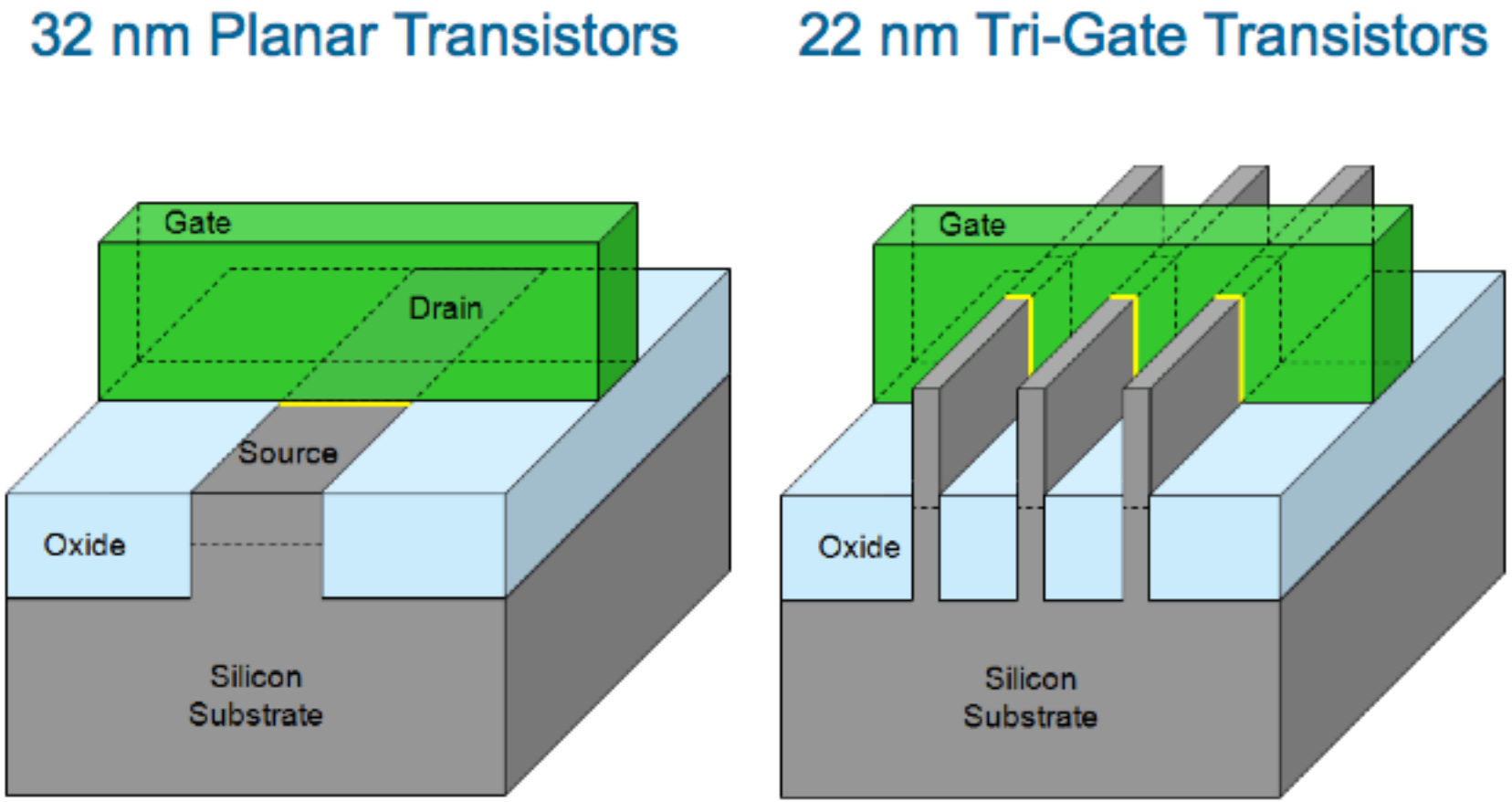
The emerging nano-technologies

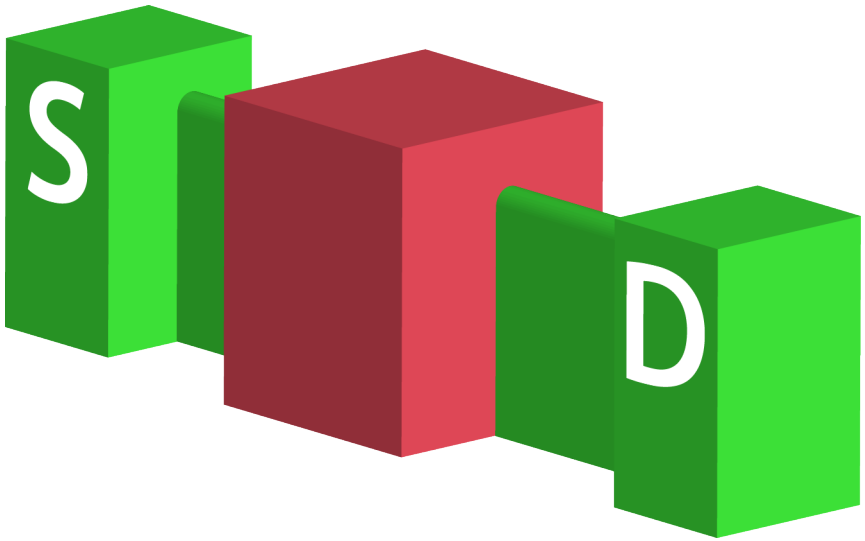
- *Enhanced* silicon CMOS is likely to remain the main manufacturing process
  - The 10nm and 7nm technology nodes are planned
- What are the candidate technologies for the 5nm node and beyond?
  - Tunneling FETs (TFET)
  - Silicon Nanowires (SiNW)
  - Carbon Nanotubes (CNT)
  - 2D devices (flatronics)
- What are the common denominators from a design standpoint?

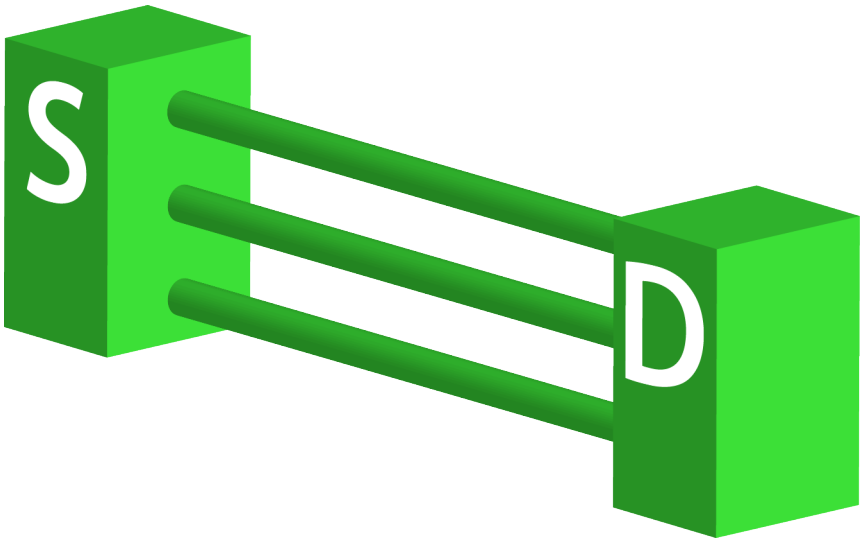
22 nm Tri-Gate Transistors



[Courtesy: M. Bohr]

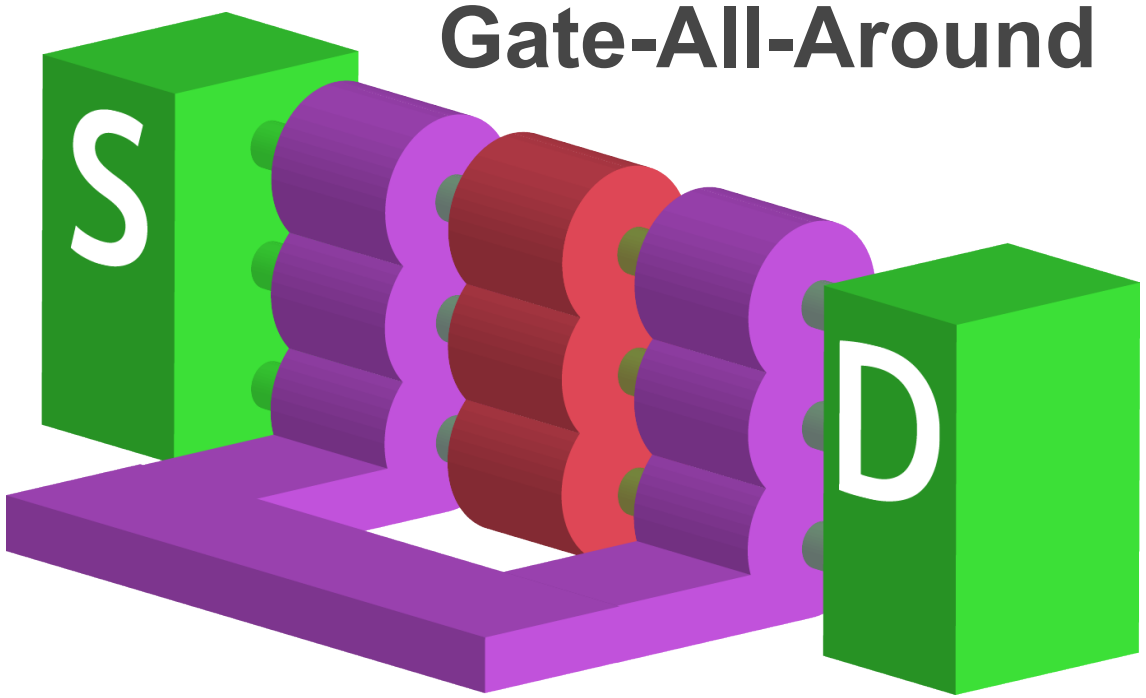
From FinFET to Nanowire FET





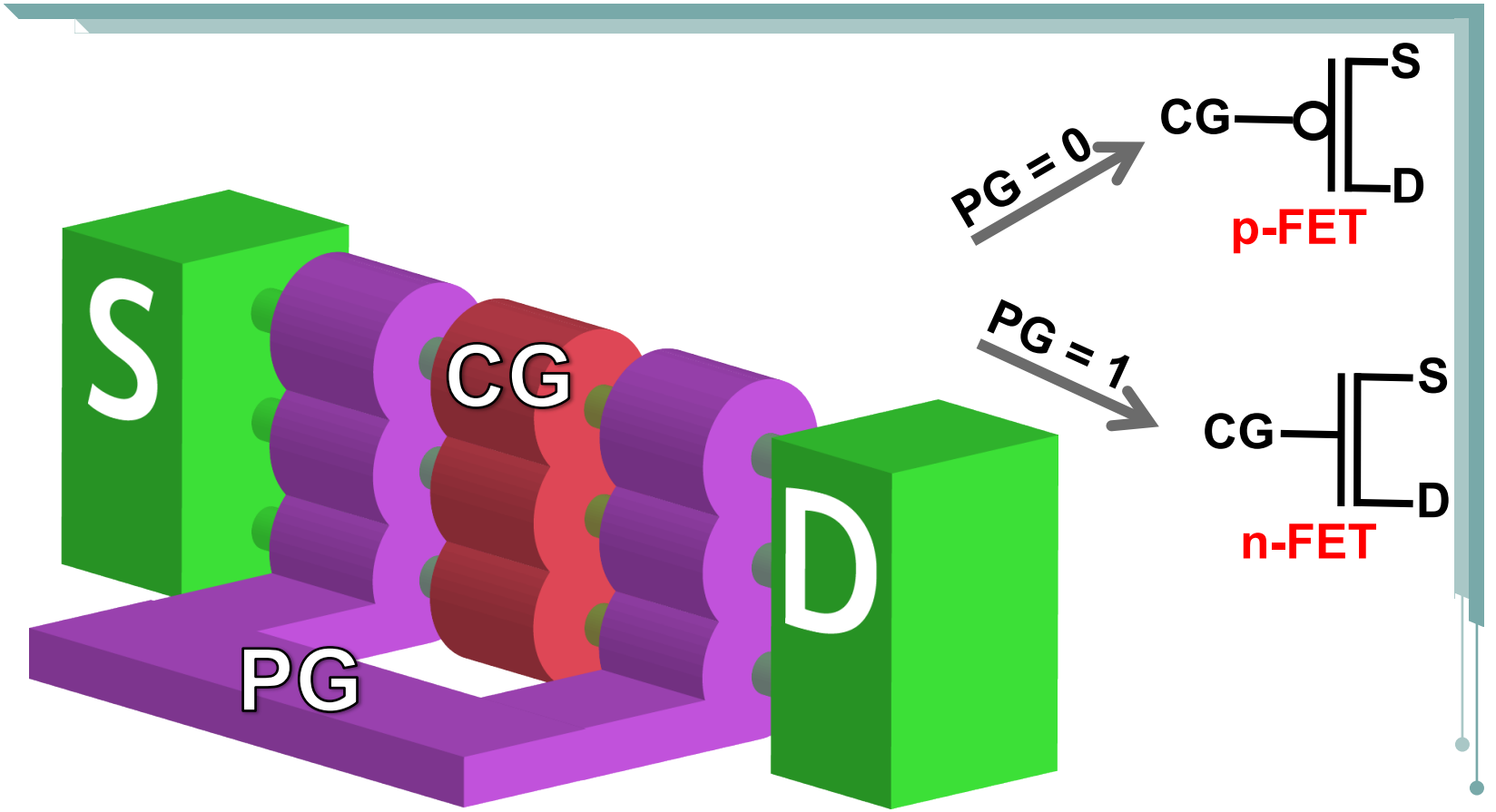
FinFET **NW FET**

Vertically-aligned Nanowire FETs



NW FET

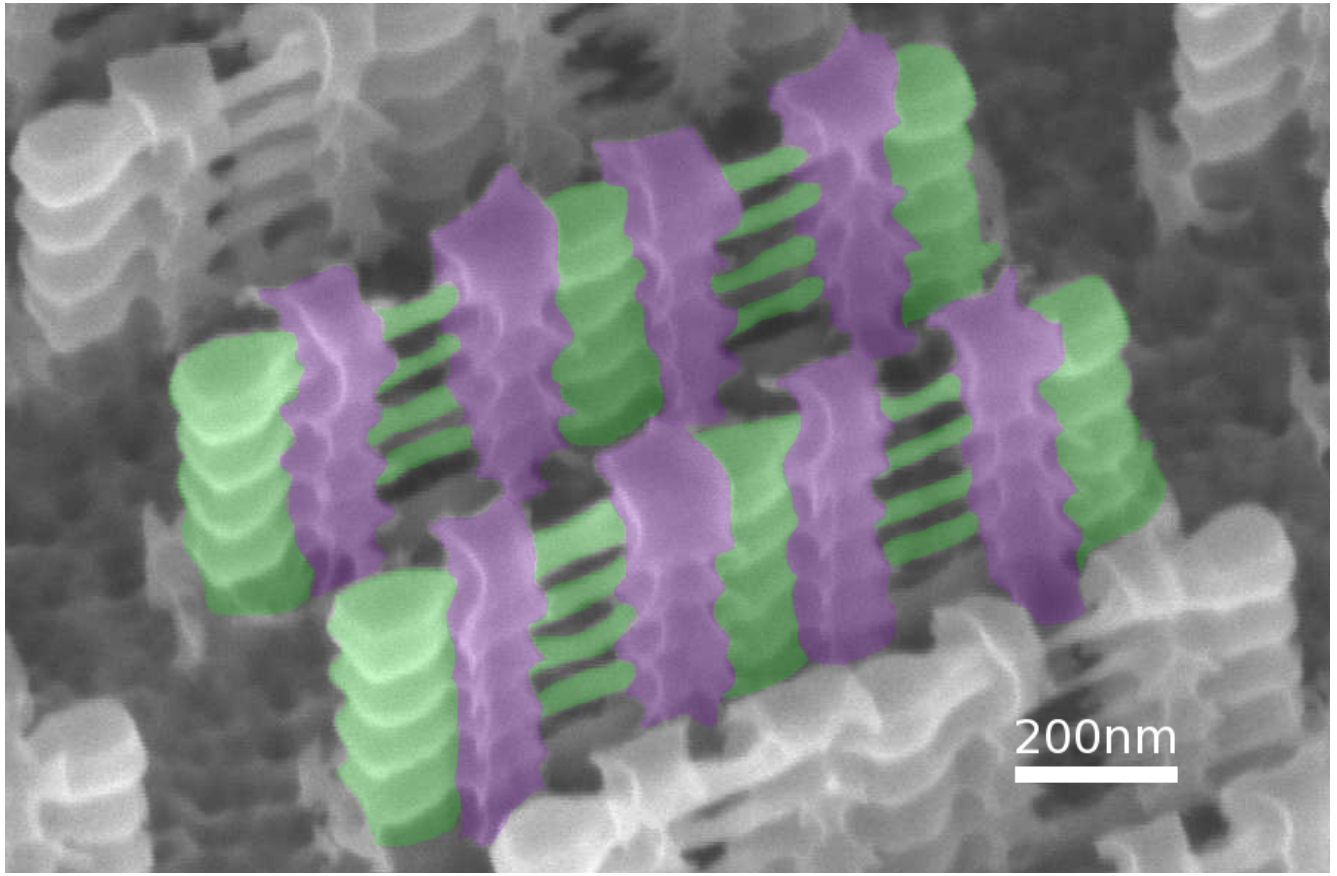
Electrostatic doping



- **Electrically program** the transistor to either **p-type** or **n-type**
- Field-effect control of the Schottky barrier

Silicon Nanowire Transistors

- Gate all around transistors
- Double gate to control polarity



[Courtesy: De Marchi, EPFL]

Silicon Nanowire Transistors

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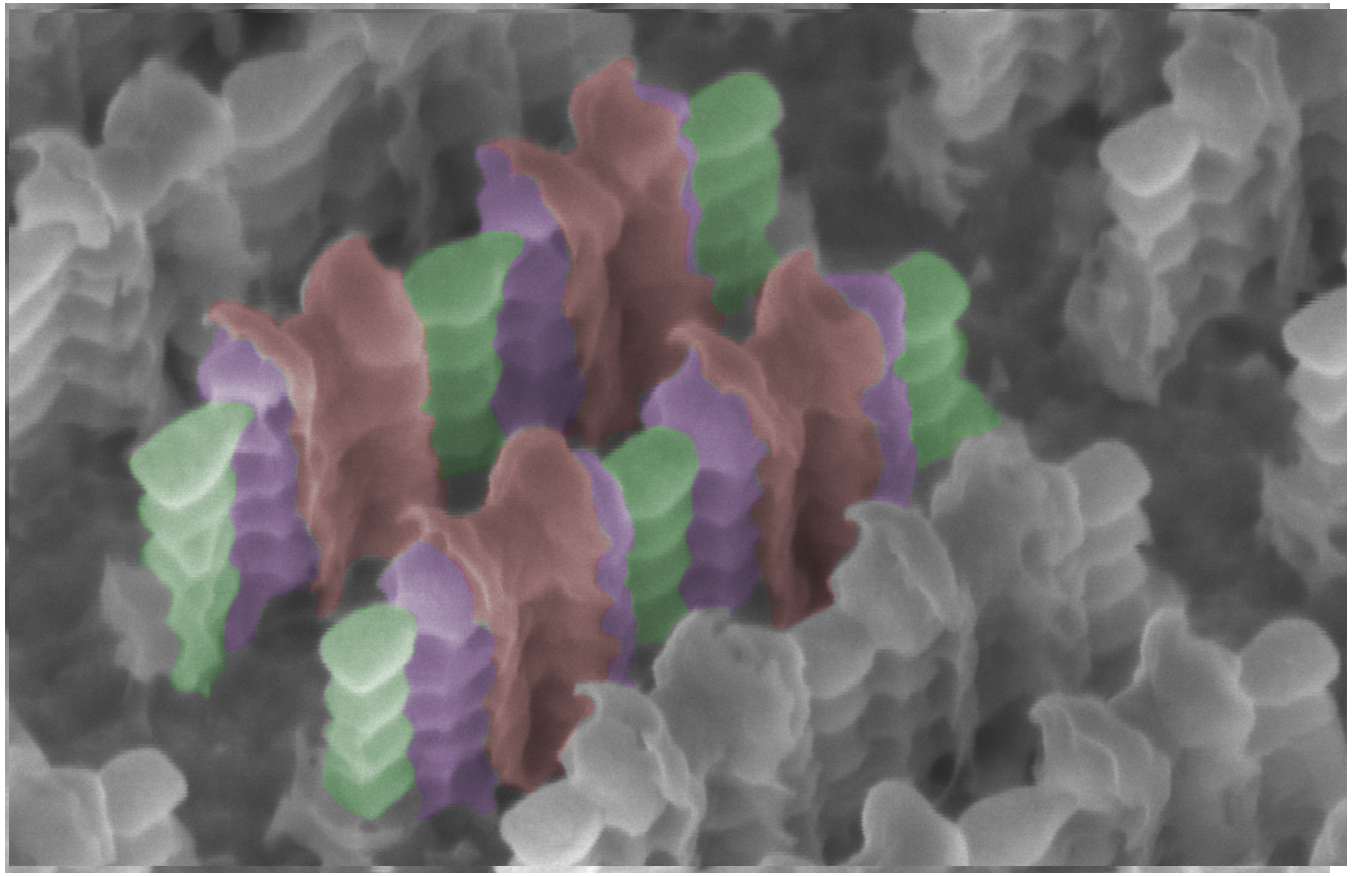
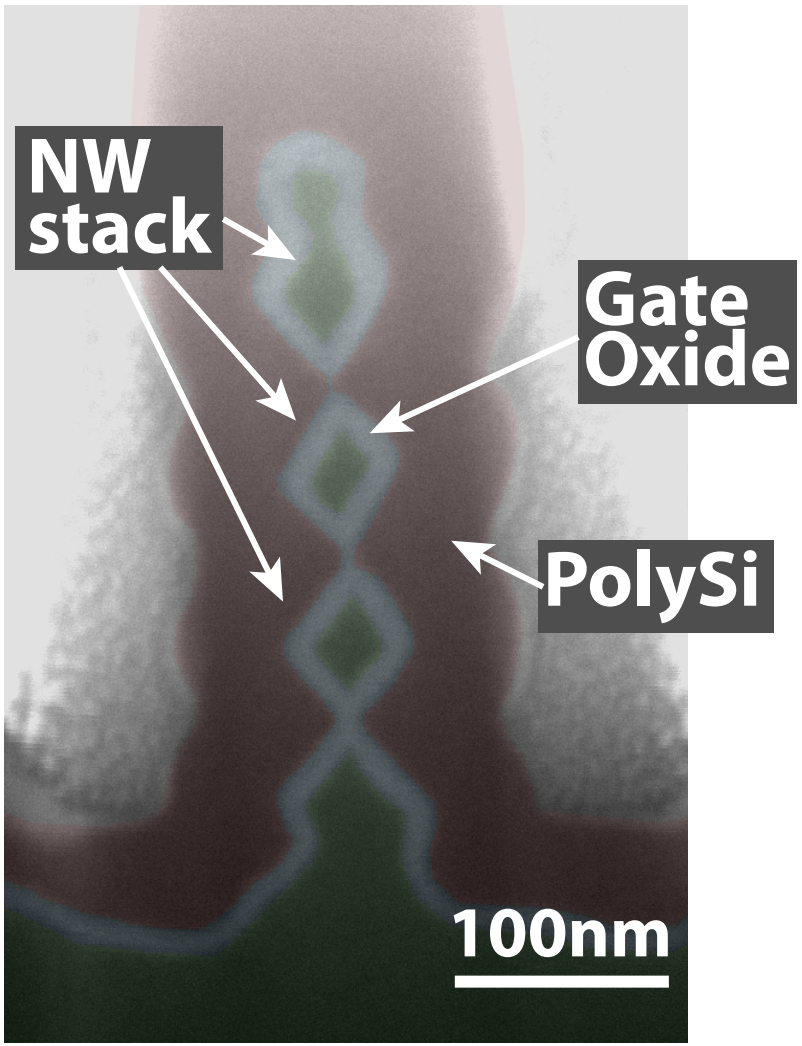
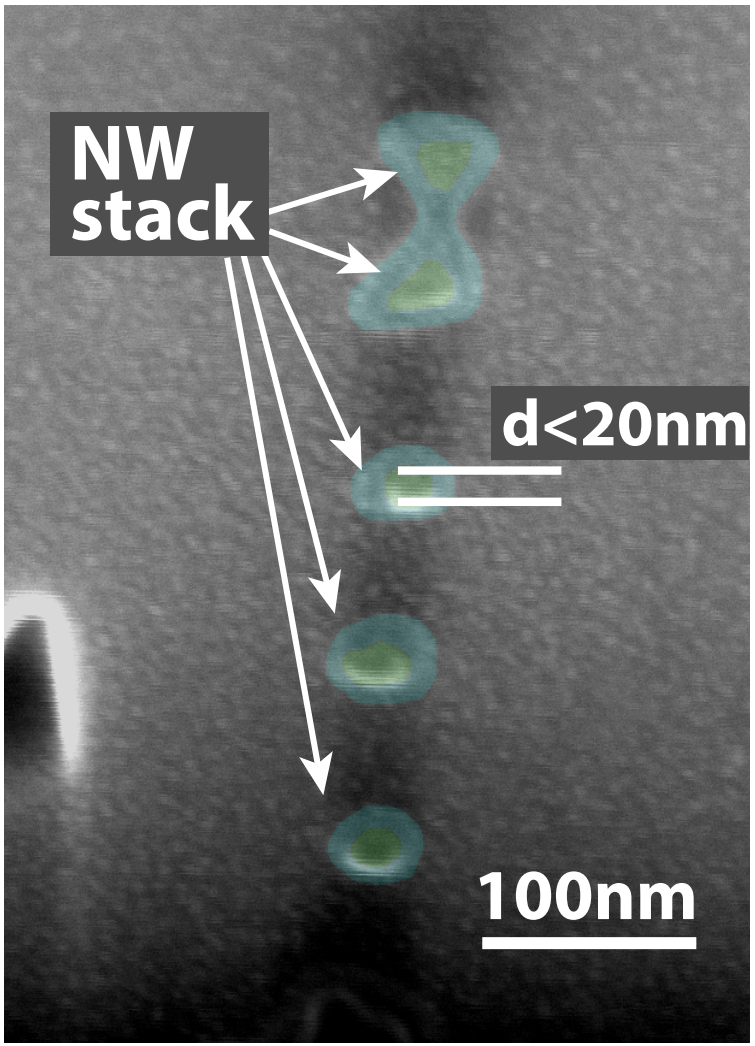


[Courtesy: De Marchi, EPFL]

Device cross sections





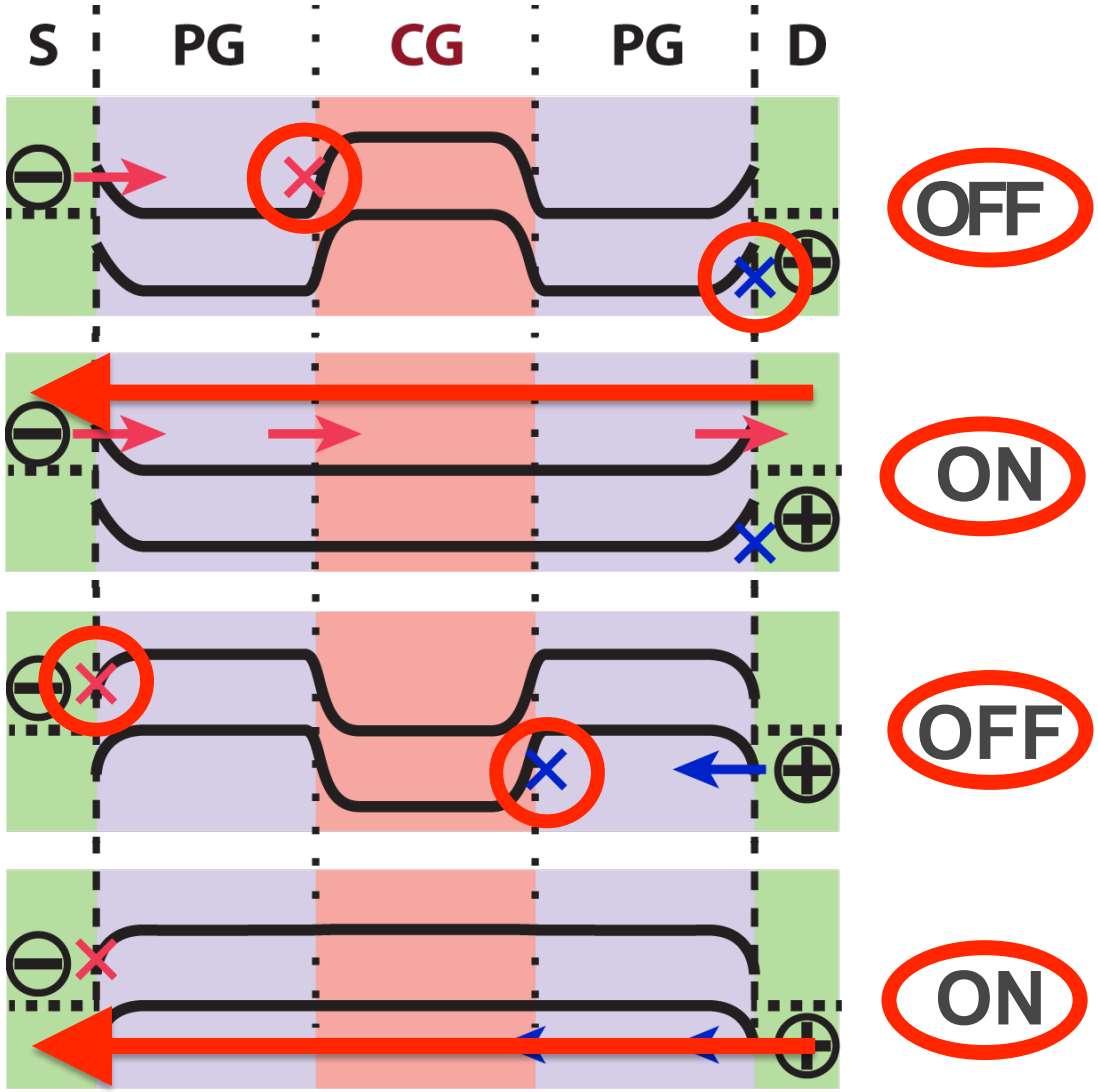
Device working principle

PG = 1→ n-type
CG = 0

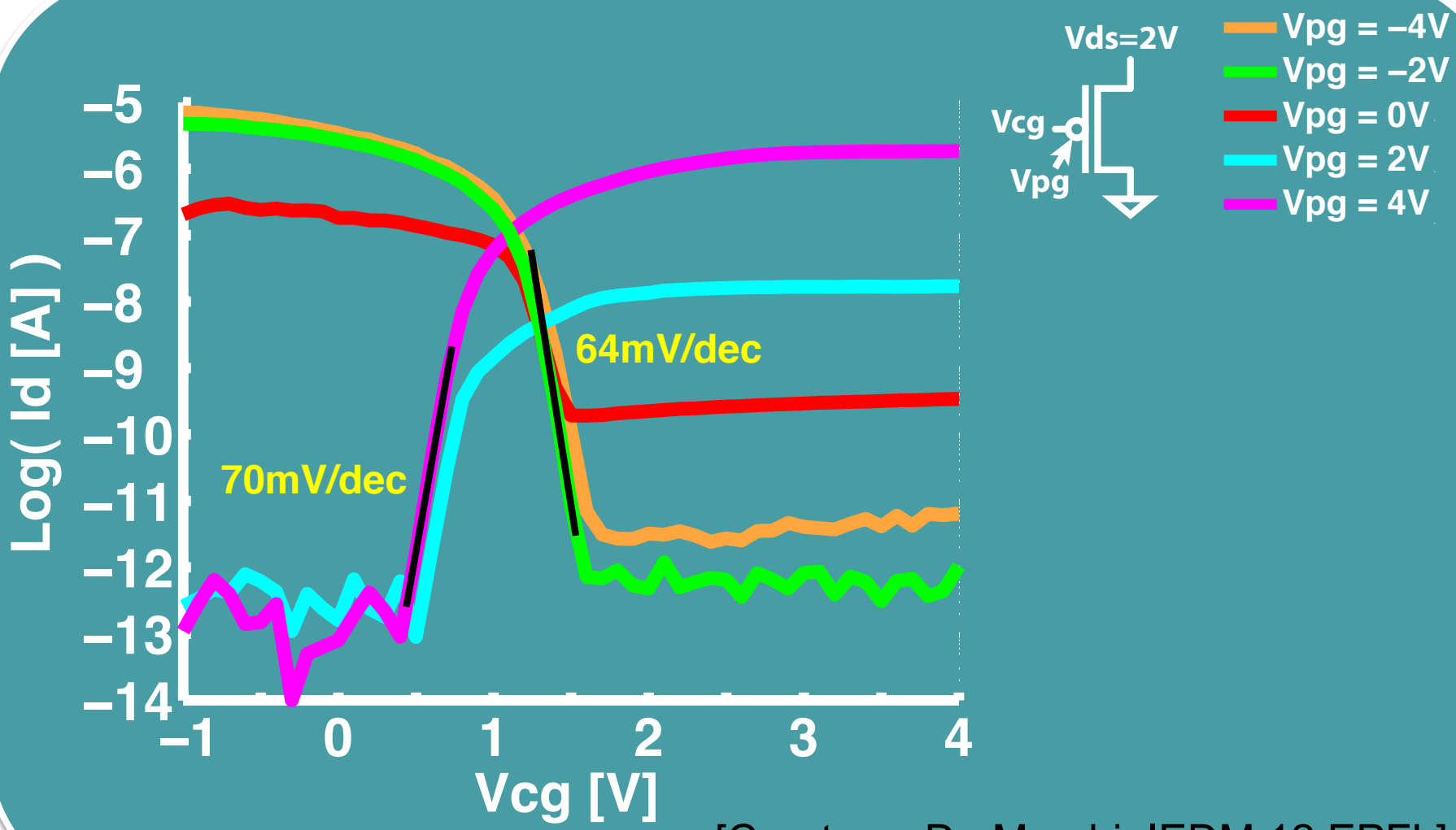
PG = 1→ n-type
CG = 1

PG = 0→ p-type
CG = 1

PG = 0→ p-type
CG = 0



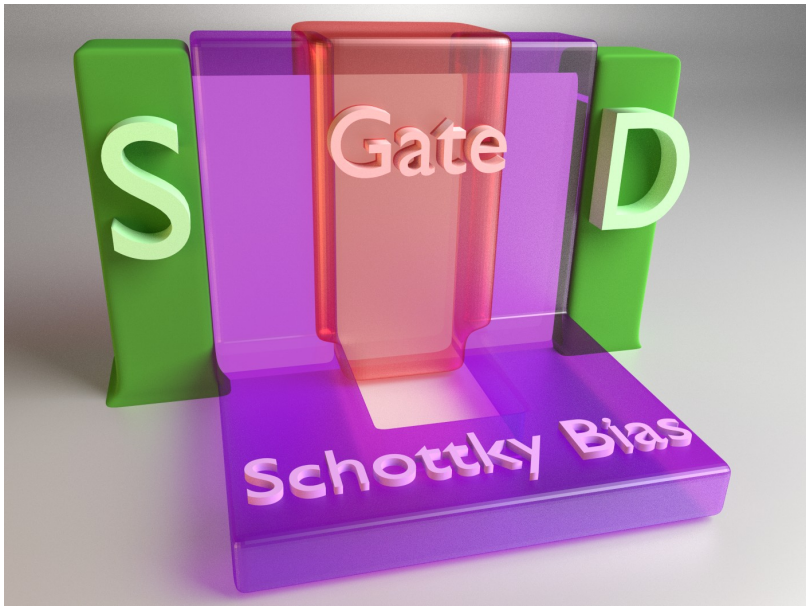
Device I_d/V_{cg}



[Courtesy: De Marchi, IEDM 12 EPFL]

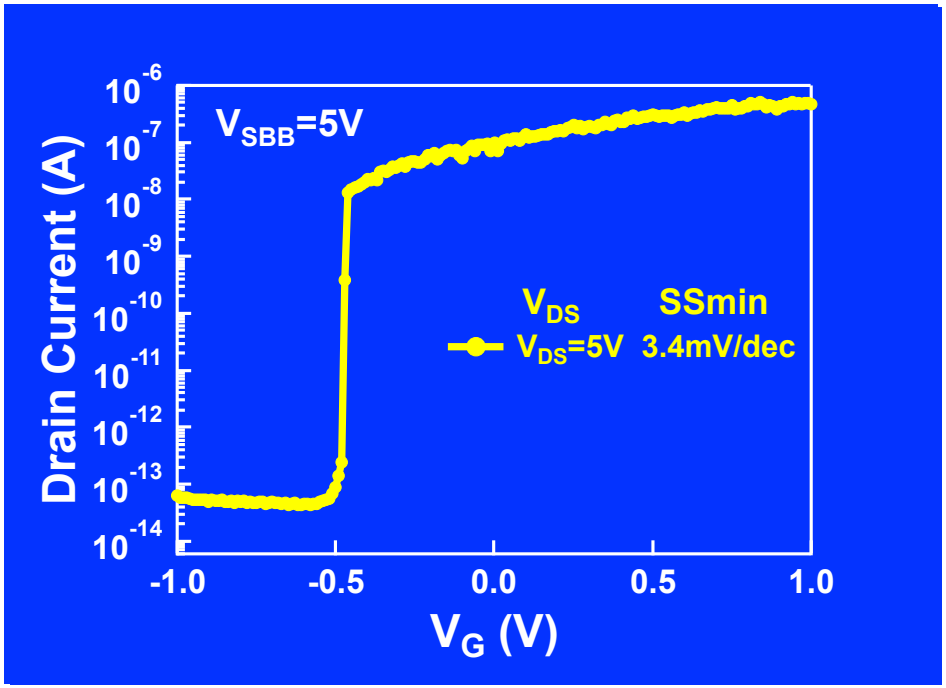
Similar devices

- Controlled devices can be realized with various materials and shapes (e.g., FINFET)
- SiNW controlled-polarity devices can be made with one polarity gate **on one side** [Heinzig]
- Polarity-gate bias can enable:
  - Steep Subthreshold
  - Multiple threshold voltages



Steep subthreshold slope devices

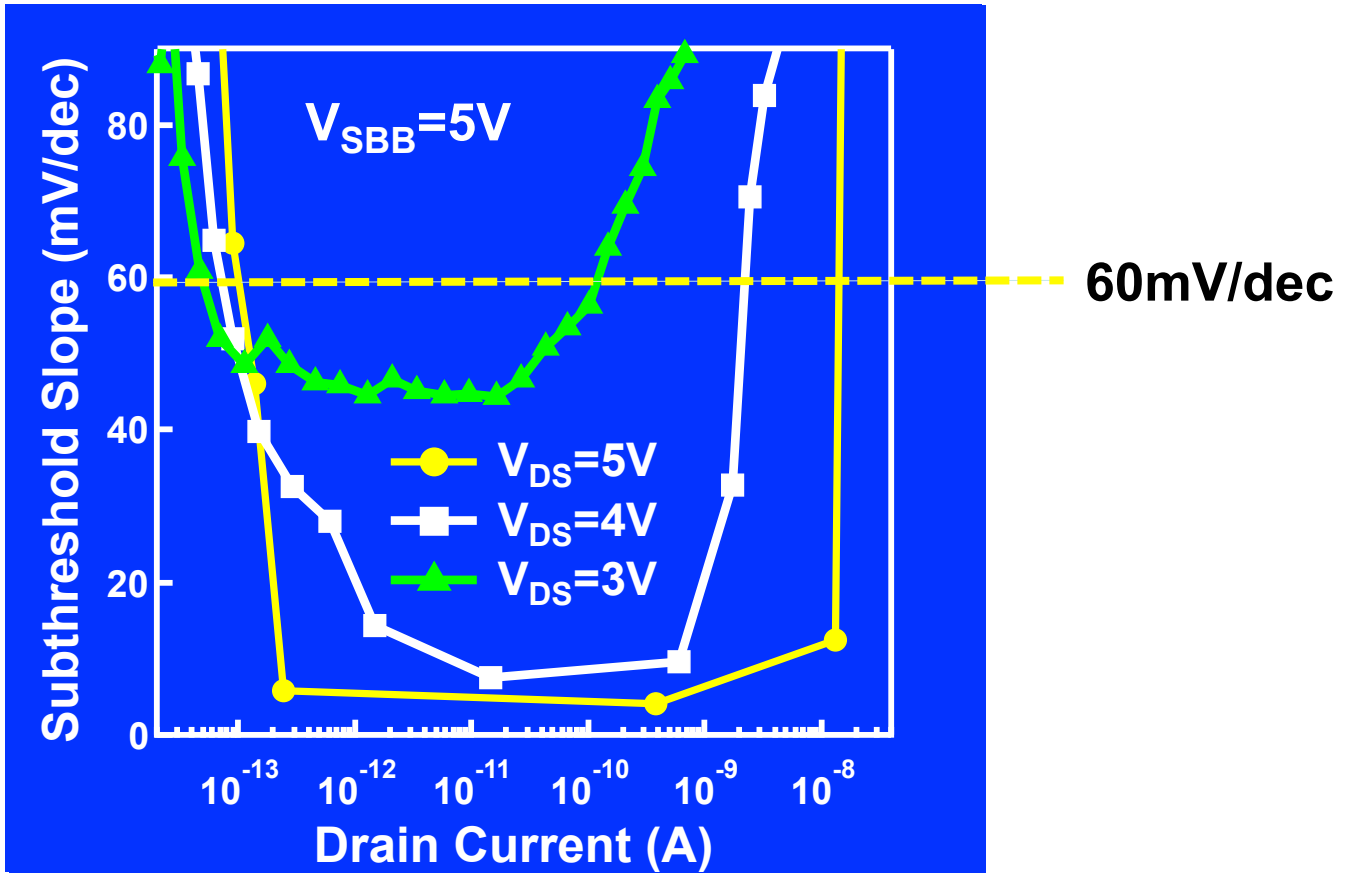
- Polarity gate at fixed voltage to create potential wells
- Barrier lowering due to carrier generation by impact ionization and accumulation in S/D well areas



[Zang –IEDM 14]

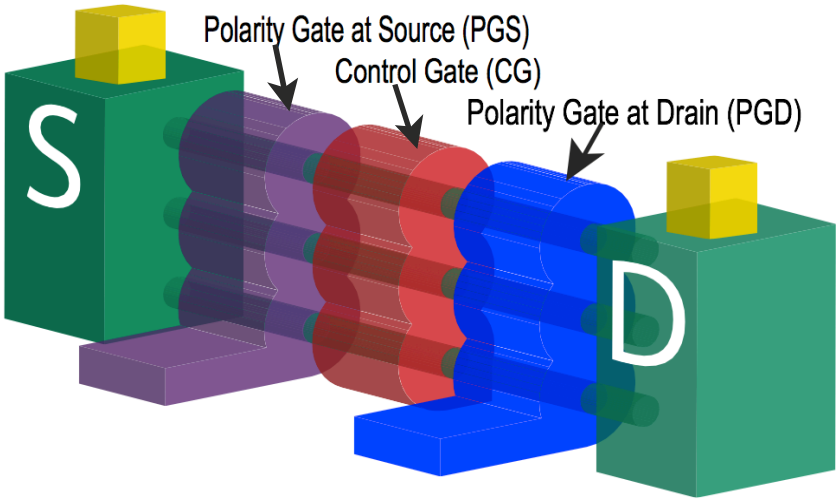
Average Subthreshold slope

- 6 mV/decade over 5 decades of current



Three-independent-gate SiNWFET

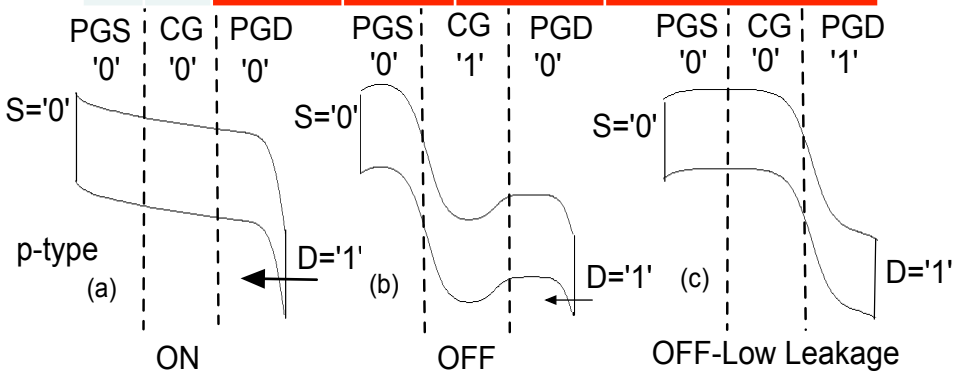
❖Structure



- **Vertically stacked nanowires**
- **3 independent gate regions**
- **Schottky barrier contacts at S/D**
- **Polarity and Vt controllability**

❖Electrostatic control

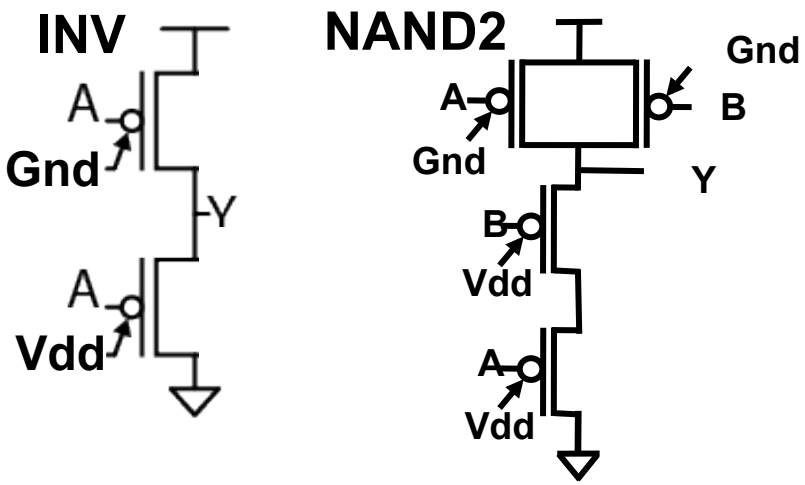
S	D	PGS	CG	PGD	State
0	1	0	0	0	ON (P-type)
		1	1	1	ON (N-type)
		0	1	0	OFF (LVT)
		1	0	1	OFF (LVT)
		0	0	1	OFF (HVT)
		0	1	1	OFF (HVT)



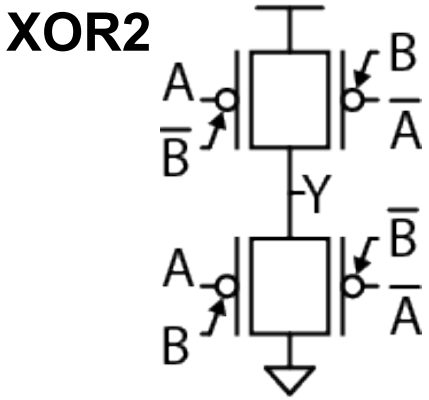
Library cell design for double-gate SiNWFETs

- Exploit complementary to achieve full swing
- Require smart local routing to compensate for extra input
- Major advantage is handling binate logic functions well (e.g., XOR)

Negative Unate functions	Binate functions

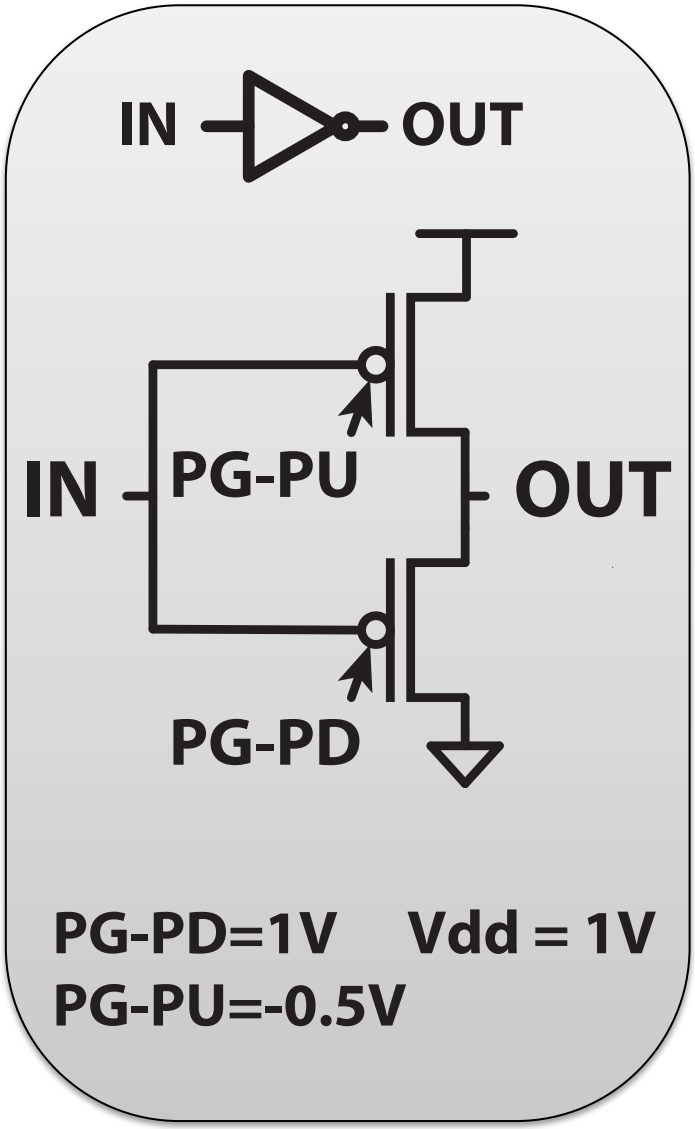


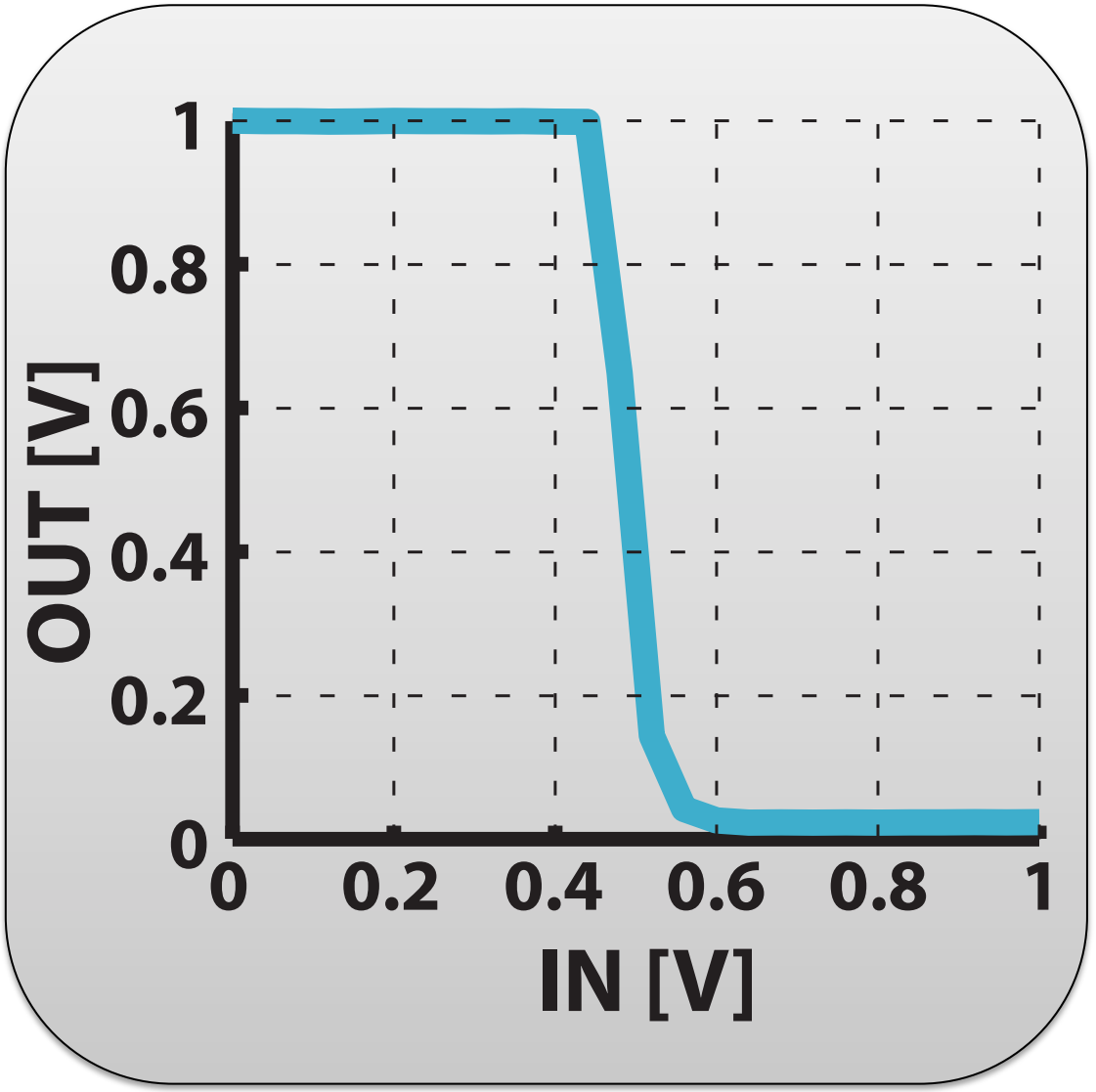
Similar to regular CMOS



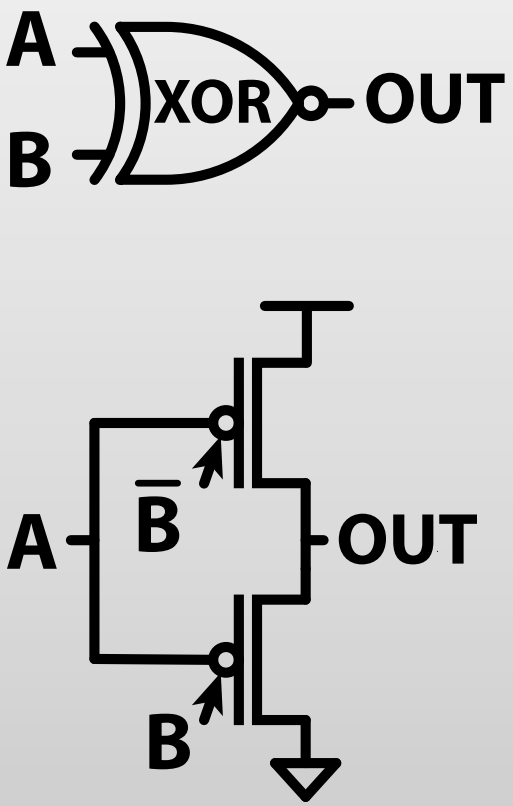
Only 4 transistors when compared to 8 transistors with a regular CMOS

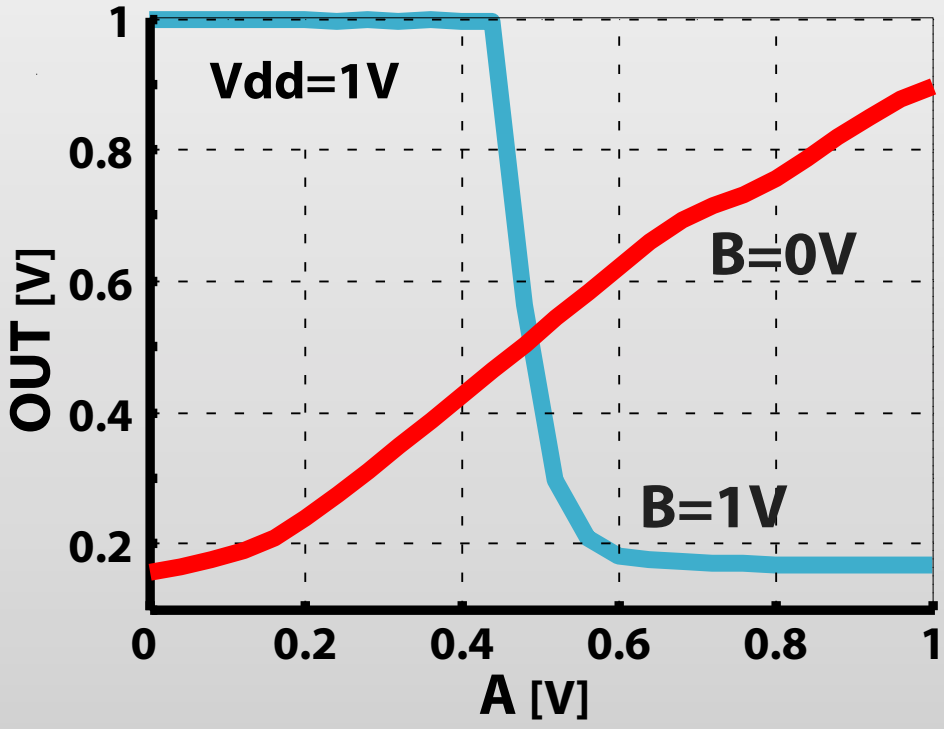
2 FET inverter configuration



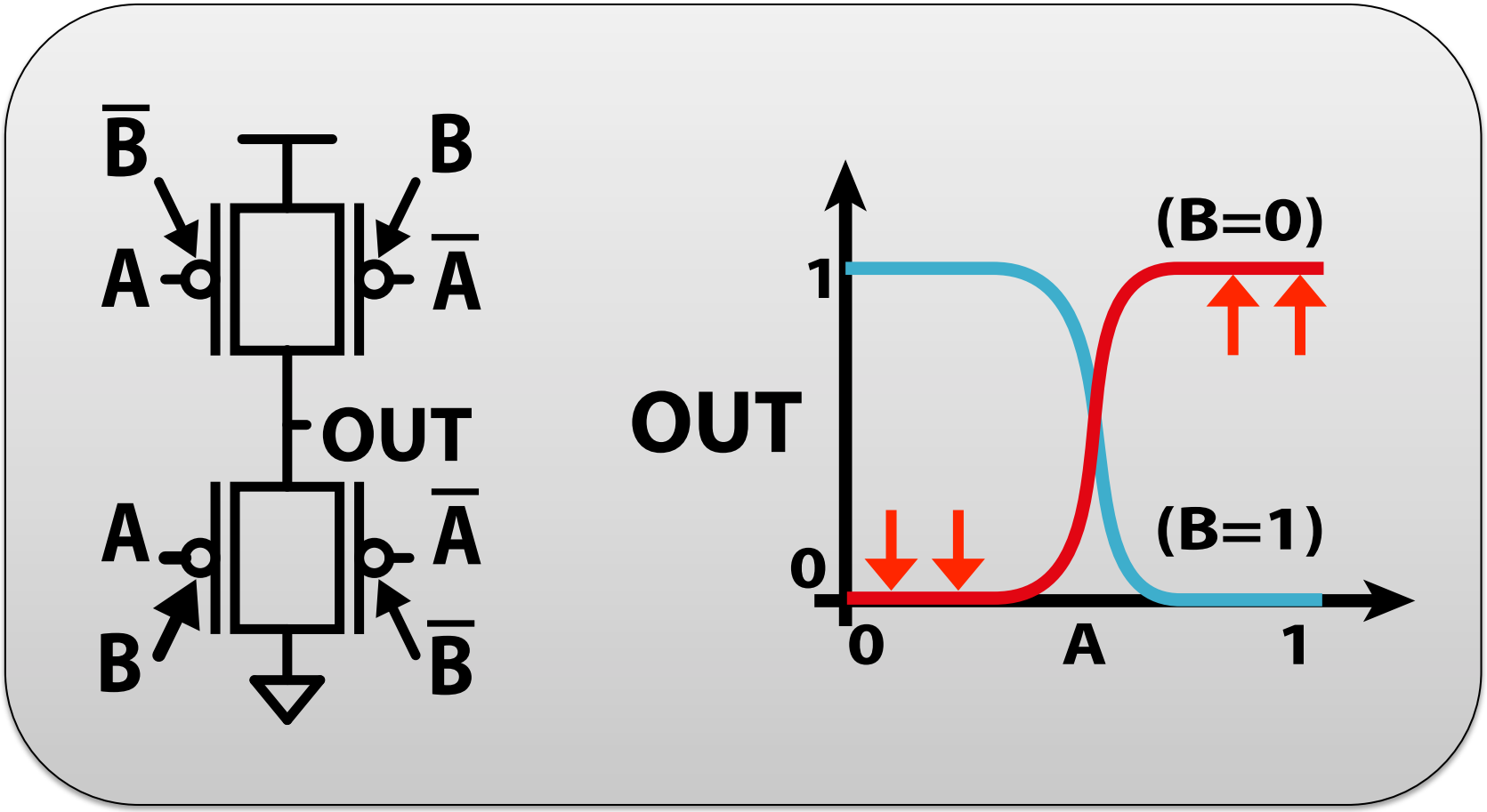


2 transistor XOR circuit

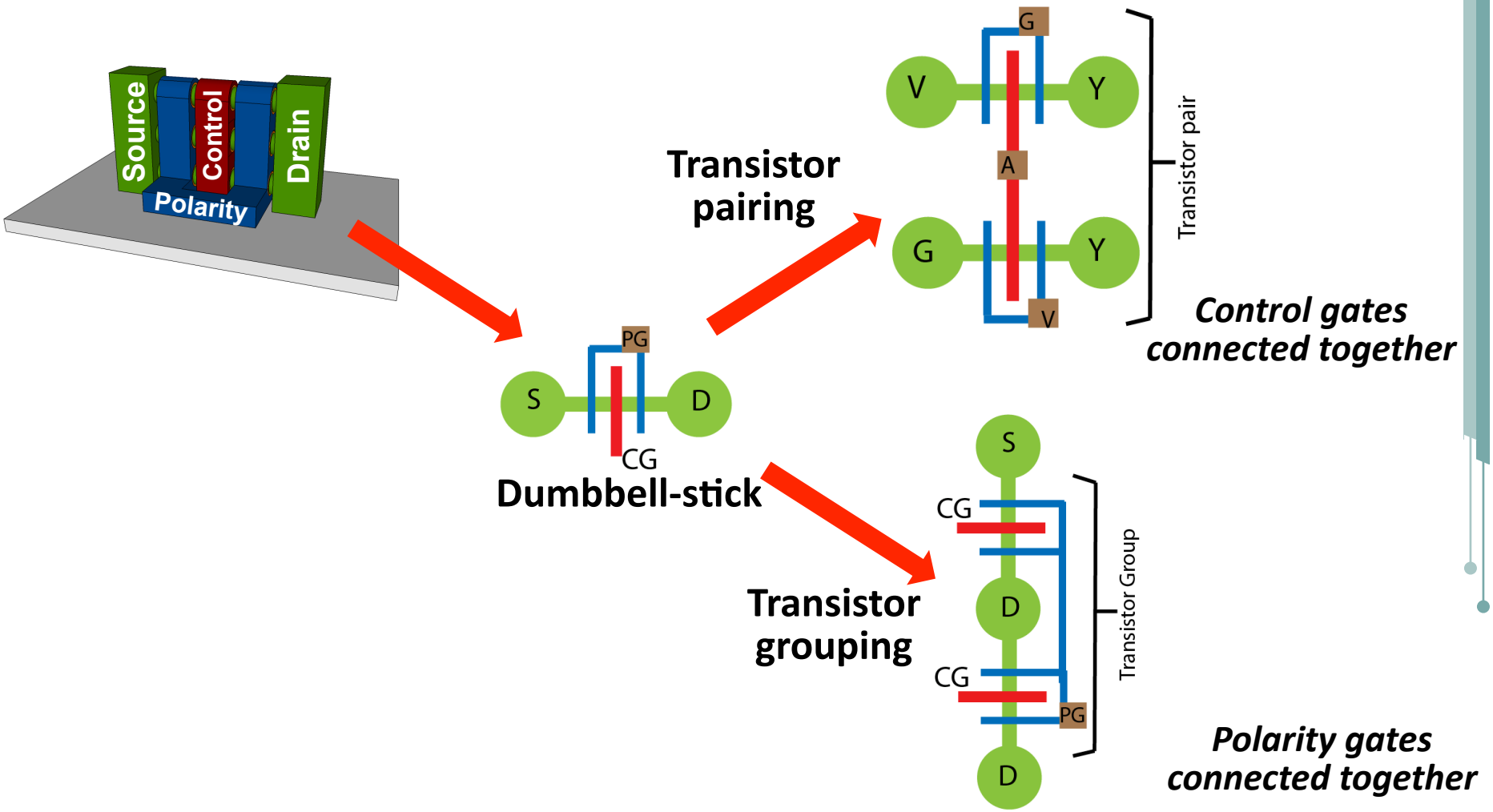




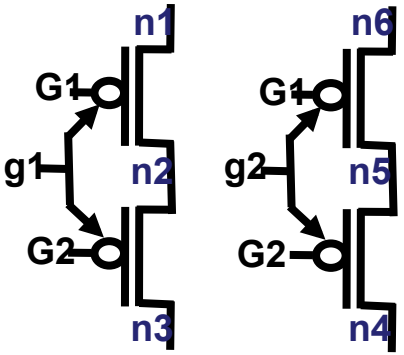
Full swing XOR circuit

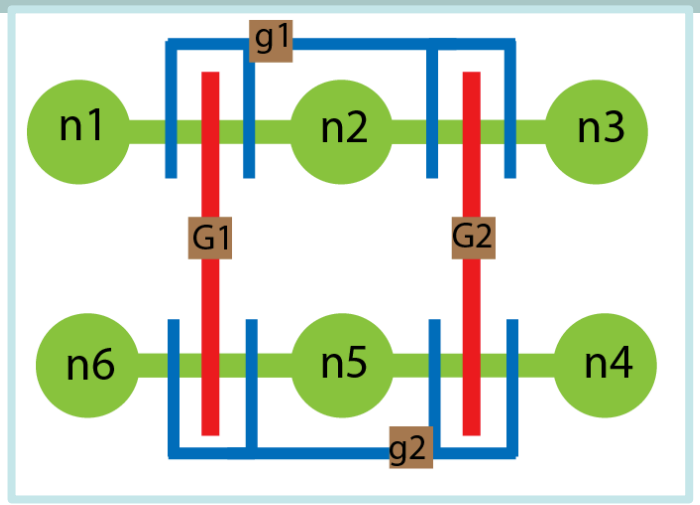


Dumbbell-stick diagrams



Layout abstraction and regularity with *Tiles*

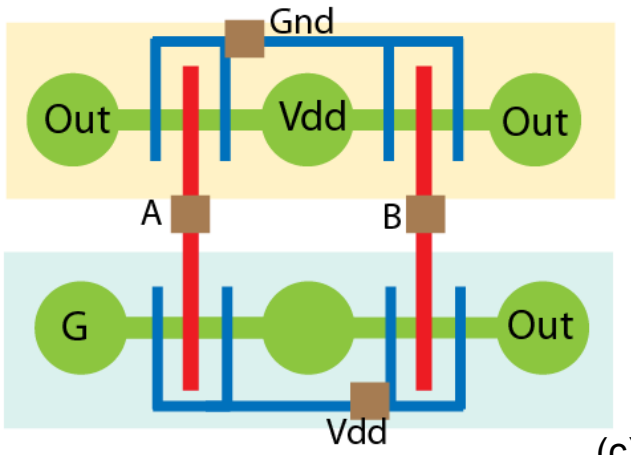




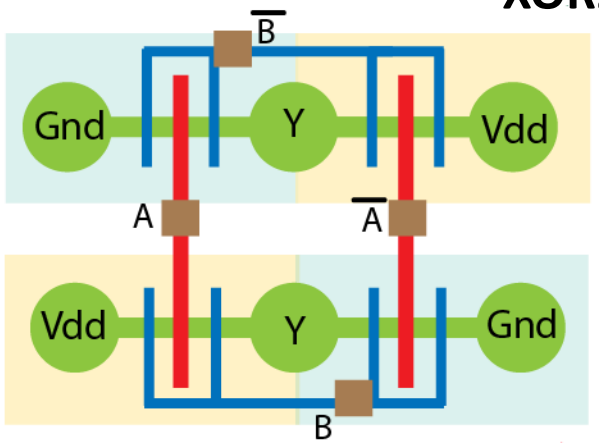
Tile

Two transistor pairs grouped together

NAND2



XOR2



[Courtesy: Bobba, DAC 12]

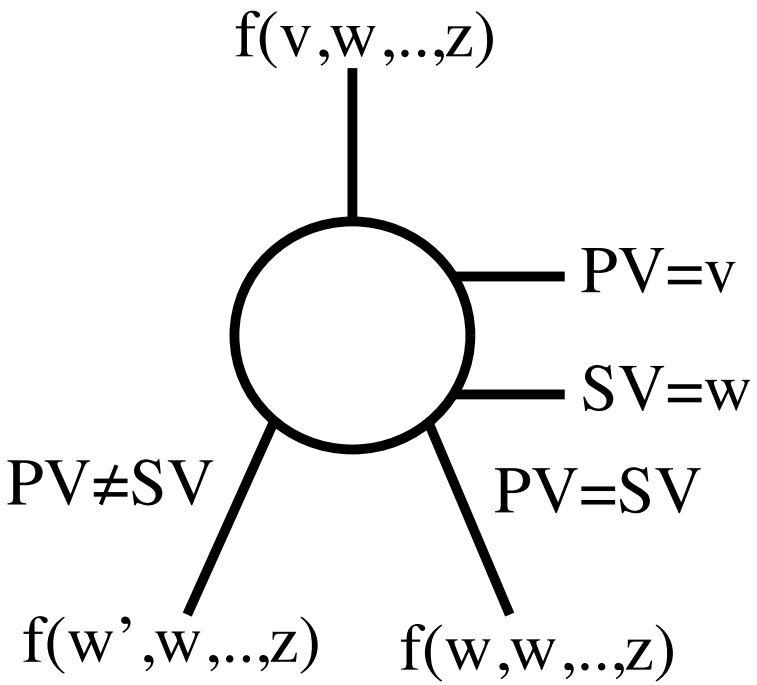
Logic level abstraction

- Three terminal transistors are switches
  - A loaded transistor is an *inverter*
- Controllable-polarity transistors compare two values
  - A loaded transistor is an *exclusive or* (EXOR)
- The intrinsic higher computational expressiveness leads to more efficient data-path design
- The larger number of terminals must be compensated by smart wiring

Biconditional Binary Decision Diagrams

- Native **canonical** data structure for logic design
- *Biconditional* expansion:

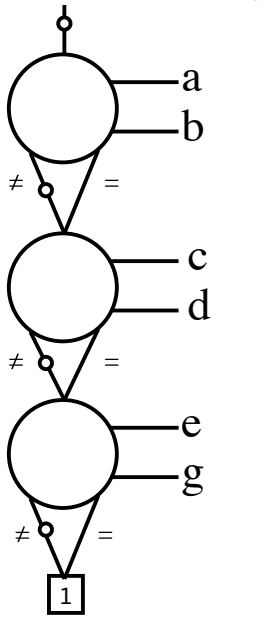
$$f(v,w,..,z) = (v \oplus w) f(w',w,..,z) + (v \overline{\oplus} w) f(w,w,..,z)$$



- Each BBDD node:
  - Has two branching variables
  - Implements the *biconditional* expansion
  - Reduces to Shannon's expansion for single-input functions

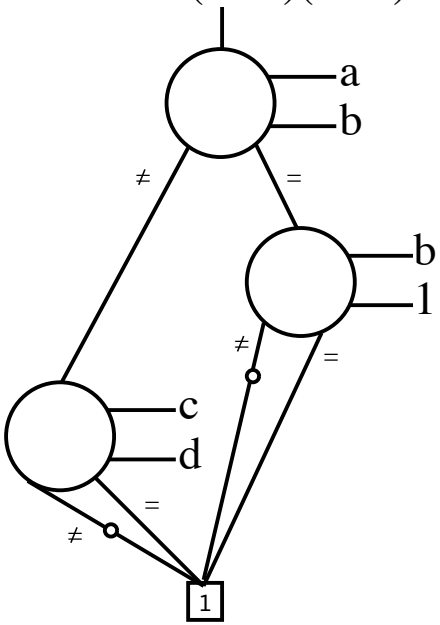
BBDD: Examples

a) f=a⊕b⊕c⊕d⊕e⊕g



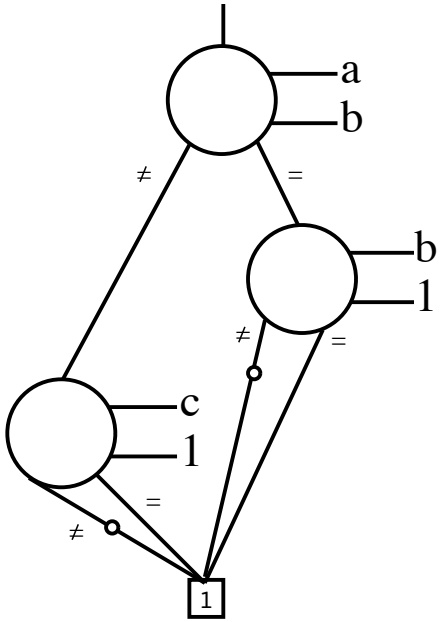
π=(a,b,c,d,e,g)

b) f=ab+(a⊕b)(c⊕̄d)



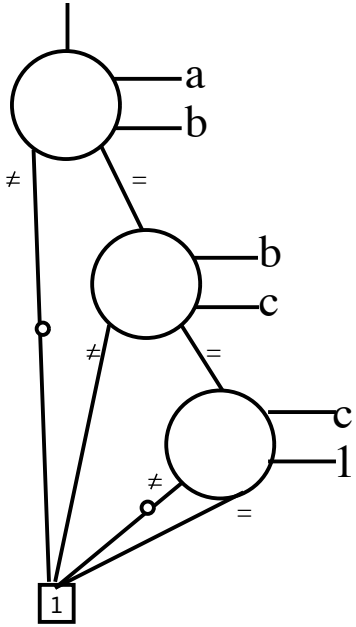
π=(a,b,c,d)

c) f=ab+bc+ac



π=(a,b,c)

d) f=(a⊕̄b)(b+c)

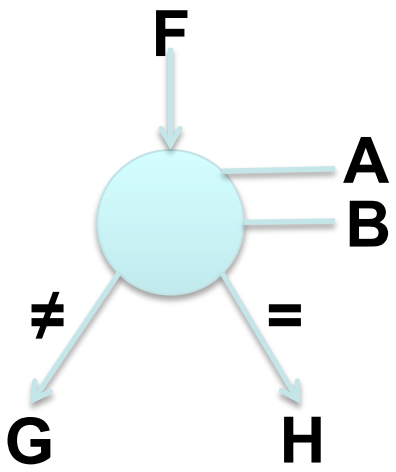


π=(a,b,c)

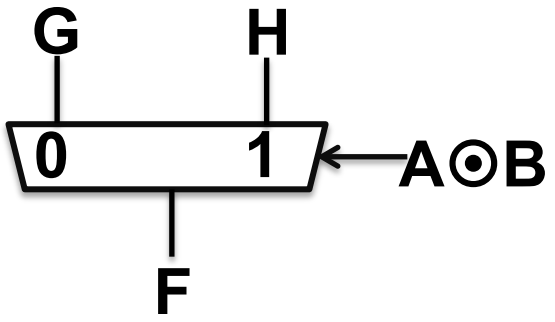
- The BDD counterparts for these examples have about 50% more nodes!

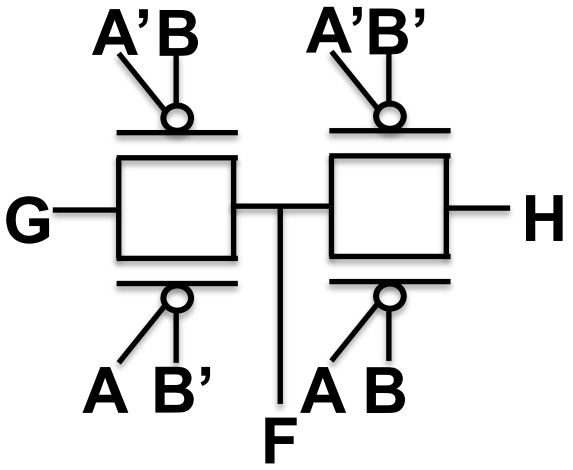
Efficient Direct Mapping of BBDD Nodes

BBDD node

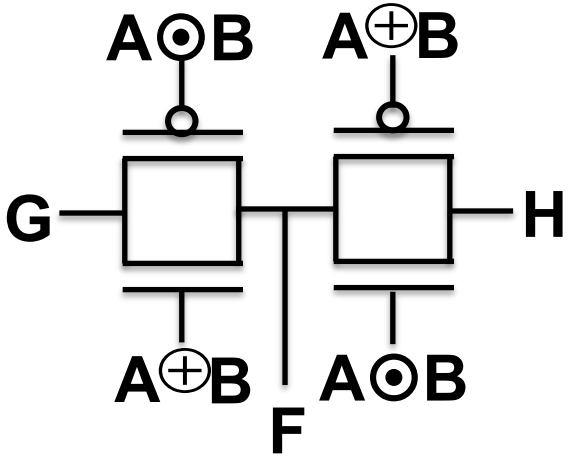


MUX driven by a XNOR





Controlled-polarity

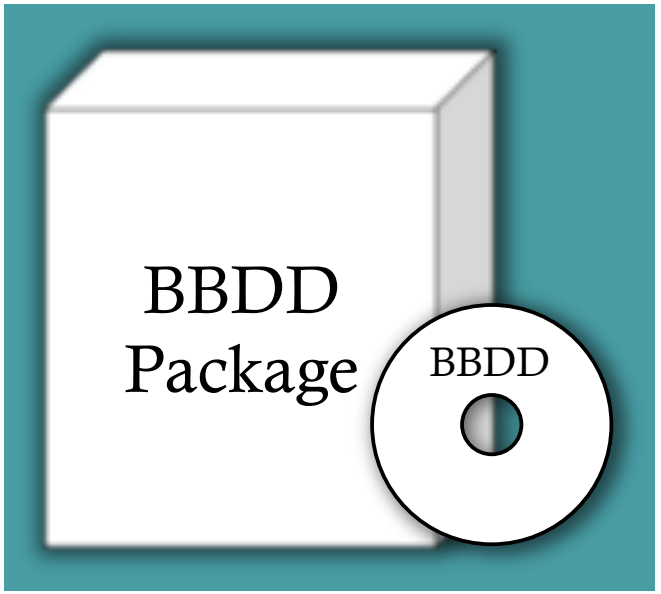


CMOS

The BBDD optimization tool

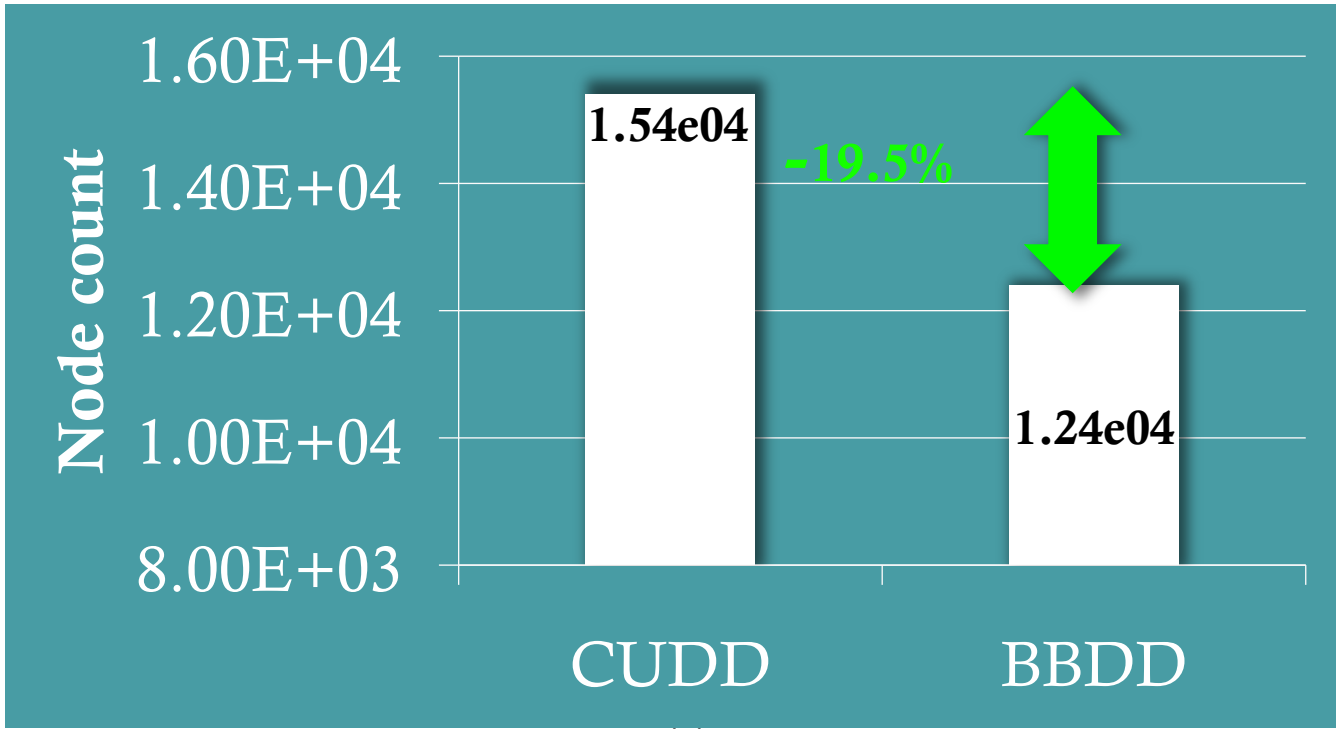
- Unique table to store BBDD nodes
- Recursive formulation of Boolean operations
- Performance-oriented memory management
- Chain variable reordering

http://lsi.epfl.ch/BBDD



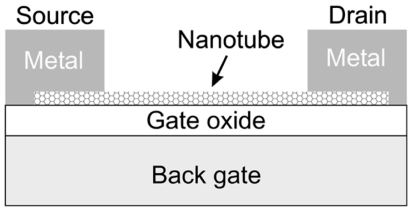
Experimental results

- We implemented a BBDD package in C language
  - Comparison with CUDD (BDD)
- Both CUDD and BBDD first build the DDs and then apply sifting (no dynamic reordering)

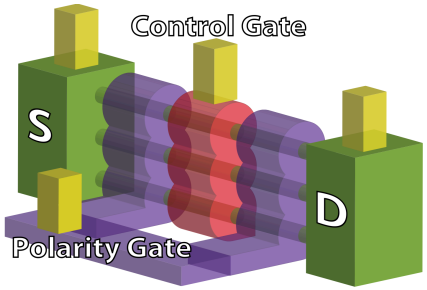


Also 1.63x speedup for arithmetic intensive circuits

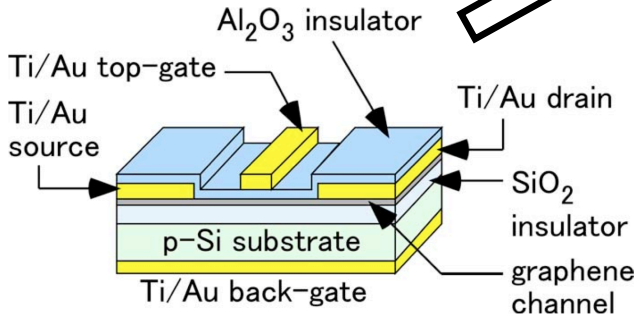
Modeling various emerging nanogates



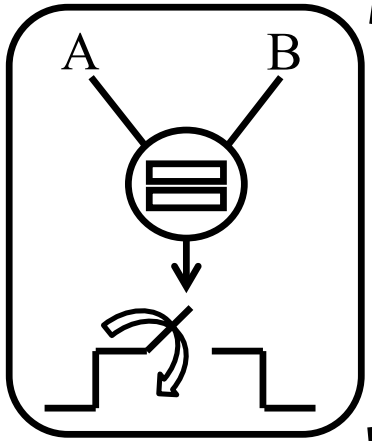
CNFETs

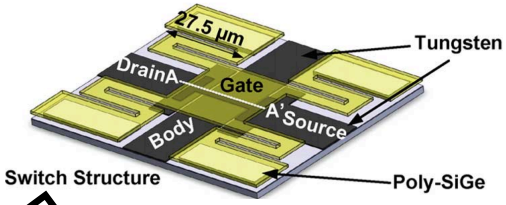


SiNWFETs

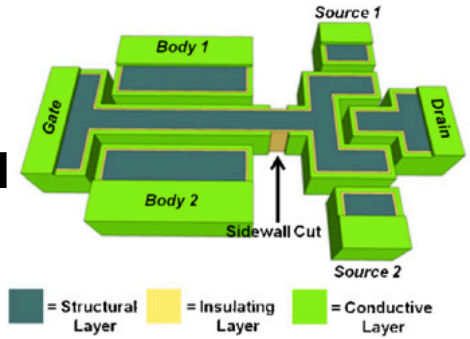


Graphene FETs

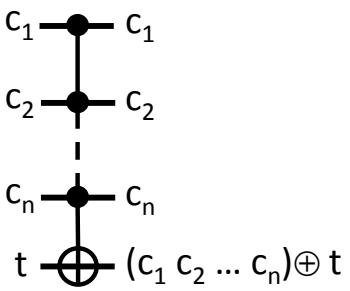




4T Nanorelays



6T Nanorelays



Reversible Logic

Conclusions

- The FINFET is the first successful 3D transistor
- FINFET evolution comprises variations:
  - Multi filament devices (NanoWires)
  - Multi gate devices
- Additional gate biasing can be used to enhance logic functionality and/or performance of devices
- Device effectiveness in constructing logic cells depends significantly on physical design
- New logic design tools are key to asses the potential use of these technologies

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